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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,777	01/11/2002	Marc Chason	CMO1533I(72804)	8364

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EXAMINER	
DOLAN, JENNIFER M	
ART UNIT	**PAPER NUMBER**
2813	8

DATE MAILED: 04/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,777	CHASON ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action is in response to the Affidavit under 37 CFR §1.131, filed 2/5/03

Response to Amendment

1. The Affidavit filed on 2/5/03 under 37 CFR 1.131 is sufficient to overcome the U.S. Patent Publication No. 2002/0119600 to Pierce reference.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites the limitation "exposing the at least one of the materials to low-temperature drying." There is insufficient antecedent basis for this limitation in the claim. For the purposes of examination, it is assumed that "drying" is replaced by –processing--, as per claim 10.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by European Patent Publication No. 0 475 022 A1 to Grube.

Regarding claim 1, Grube discloses a method comprising: providing an interposer (16) having at least one semiconductor die (chip 10) attached to a first side thereof (figure 2); and prior to placing the interposer on a printed wiring board (module 12), disposing an underfill material (18) on at least a portion of a second side thereof (figure 2).

Regarding claim 14, Grube further discloses providing a plurality of interposers disposed substantially co-planar to one another, wherein at least some of the interposers each have at least one semiconductor die attached to one side thereof (see column 2, lines 32-58).

Regarding claim 15, Grube discloses providing a plurality of singulated interposers (column 2, lines 55-58).

Regarding claim 16, Grube discloses providing a panel comprised of a plurality of interposers (column 2, lines 50-55).

Regarding claim 17, Grube discloses disposing an underfill material on at least a portion of the second side of at least some of the plurality of interposers (underfill is provided on the entire interposer sheet; see column 5, lines 23-39).

Regarding claim 18, Grube discloses after disposing the underfill (as in column 5, lines 23-29), singulating the interposers to provide singulated interposers (column 6, lines 5-18; figure 2).

6. Claims 1-4, 21, 22, 25, 26, and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication No. 2001/0038144 A1 to Grigg.

Regarding claim 1, Grigg discloses a method comprising: providing an interposer (20) having at least one semiconductor die (32) attached to a first side thereof (figures 7, 10-14); wherein prior to placing the interposer on a printed wiring board (see paragraph 0008, PWB equivalent to circuit board/carrier substrate), disposing an underfill material (52) on at least a portion of the second side thereof (figures 7, 10-14; also see paragraph 0059, lines 26-31).

Regarding claim 2, Grigg discloses providing an interposer having at least one interface electrode disposed on the second side thereof (46).

Regarding claim 3, Grigg discloses providing an interposer having at least one interface electrode comprising a solder ball disposed on the second side thereof (figures 7 and 10-14).

Regarding claim 4, Grigg discloses adding at least one interface electrode to the second side of the interposer (paragraph 0071).

Regarding claim 21, Grigg discloses a method comprising: providing a printed wiring board (see paragraph 0008); providing at least one interposer (10) having: a first side having at least one semiconductor die (32) affixed thereto (figures 7, 10-14); a second side having an underfilling material (52) disposed thereon (figures 7 and 10-14); and at least one interface

electrode (46) at least partially exposed through the underfilling material (figures 7 and 10-14); and disposing the at least one interposer on the printed wiring board (paragraph 0008).

Regarding claim 22, Grigg discloses that the interface electrode is a solder ball (figures 7 and 10-14).

Regarding claim 25, Grigg discloses a device comprising: a pre-placement interposer (10) having: a first side having at least one semiconductor die (32) affixed thereto (figures 7 and 10-14); and a second side having: an underfilling material (52) disposed thereon; and at least one interface electrode (46) at least partially exposed through the underfilling material (figures 7 and 10-14).

Regarding claim 26, Grigg discloses means for physically and electrically coupling a semiconductor die to a printed wiring board (in the form of solder balls 46; see paragraph 0059, lines 26-31; paragraph 0008).

Regarding claim 28, Grigg discloses that the second side has a plurality of interface electrodes at least partially exposed through the underfilling material (figures 7 and 10-14).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grube in view of U.S. Patent No. 5,251,266 to Spigarelli et al.

Regarding claim 19, Grube fails to disclose placing singulated interposers into a carrier to facilitate subsequent placement of the singulated interposers on a printed wiring board.

Spigarelli discloses placing singulated IC devices in a carrier (column 4, lines 1-4) to facilitate subsequent placement of the singulated devices on a printed wiring board (column 8, lines 38-45; column 13, lines 37-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Grube, such that singulated interposers are placed into a carrier, as taught by Spigarelli. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to place the singulated interposers into a carrier, so that the carrier features can be utilized to determine the position of each interposer, and thus allow for greater accuracy of placement onto a printed wiring board (Spigarelli, column 13, lines 37-68).

Regarding claim 20, Grube fails to disclose placing at least some of the singulated interposers into at least one of a tape and reel carrier, a waffle pack, and a matrix tray.

Spigarelli discloses placing IC devices into a matrix tray (column 4, lines 1-4; column 8, lines 38-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Grube, such that the singulated interposers are placed in a matrix tray, as taught by Pierce. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to place the interposers in a matrix tray, so that the position of each interposer is a known parameter, thus enabling automated pick

and place bonding to a printed wiring board (Spigarelli, column 8, lines 38-45; column 13, lines 37-68).

9. Claims 1 and 4-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,335,571 to Capote et al. (cited by applicant) in view of U.S. Patent No. 5,258,648 to Lin.

Regarding claim 1, Capote discloses a method comprising: providing a semiconductor die (100, 10), and prior to placing the die on a printed wiring board (101, 20), disposing an underfill material (112, 37) on at least a portion of a second side thereof (figures 10-27).

Capote fails to disclose using an interposer with a semiconductor die attached to a first side thereof in place of using only a semiconductor die.

Lin discloses using an interposer (22) with a semiconductor die (12) attached to a first side thereof (figures 2 and 4; column 2, lines 39-65; column 3, lines 12-25; column 4, lines 49-68), rather than using only a semiconductor die, for attachment to a printed wiring board.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Capote, such that an interposer having at least one semiconductor die attached to a first side thereof is used in place of only a semiconductor die, as taught by Lin. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an interposer with a semiconductor die in place of just a semiconductor die for bonding to a PWB, because Lin teaches that using an interposer allows for the thermal expansion compensation through use of an underfill disposed between the interposer and PWB, while still allowing a semiconductor die to be reworked or

removed from the assembly (Lin, column 2, lines 39-65; column 3, line 55 – column 4, line 20). The combination of Capote and Lin allows a semiconductor die to be mounted on the PWB, burned in, tested, and removed if defective, without permanently attaching a defective die to the assembly (also see Lin, column 1, line 60 – column 2, line 21).

Regarding claims 4 and 5, Capote (as modified by Lin, supra) discloses the method steps of adding at least one interface electrode (30) to the second side of the interposer after disposing the underfill material (37; figures 19-21).

Regarding claim 6, Capote discloses disposing an underfill material on a portion of the second side thereof while simultaneously providing at least one aperture in the underfill material (column 10, lines 57-58; column 11, lines 18-21).

Regarding claim 7, Capote (as modified by Lin, supra) discloses adding at least one interface electrode (30) in the at least one aperture (figures 19-21).

Regarding claim 8, Capote discloses forming at least one aperture (38) in the underfill material (37), and adding at least one interface electrode (30) in the at least one aperture (figures 19-21).

Regarding claim 9, Capote discloses disposing an underfill including a plurality of material layers (column 4, lines 18 – 29; column 5, lines 10-36).

Regarding claims 10 and 11, Capote discloses exposing at least one of the material layers to low-temperature processing/drying (curing would inherently cause drying; column 12, lines 1-17; column 15, lines 1-7; column 5, line 32).

Regarding claim 12, Capote (as modified by Lin, supra) discloses removing at least a portion of the underfill material to expose at least a portion of at least one interface electrode (column 9, lines 59 – 62).

Regarding claim 13, Capote discloses using grinding or abrasion to expose the electrode (column 9, lines 59 – 62).

10. Claims 23, 24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grigg in view of U.S. Patent No. 5,985,456 to Zhou et al. (cited by applicant).

Regarding claims 23 and 24, Grigg fails is silent as to any processing or heating of the interposer on the printed wiring board.

Zhou discloses that a flip chip is further processed on a printed wiring board by heating to at least partially harden the underfilling material (column 10, lines 16-33; 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify in the method of Grigg that the interposer is further processed by heating, to at least partially harden the underfilling material, as taught by Zhou. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to heat the interposer on the printed wiring board, in order to cause the solder to reflow, such that a solid electrical connection is made between the solder balls and the PWB, as well as to harden the adhesive underfill, such that a high strength bond between the PWB and interposer is created (see Zhou, column 10, lines 16-65).

Regarding claim 26, Grigg is silent as to whether the underfilling material comprises adherence means for physically coupling the interposer to a printed wiring board.

Zhou discloses an underfilling material with adherence means for coupling the device to a printed wiring board (column 10,lines 1-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the underfilling material of Grigg comprises adherence means for physically coupling the interposer to a printed wiring board, as suggested by Zhou. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an adhesive underfilling, so that the interposer can be solidly and strongly bonded to the PWB substrate (see Zhou, column 10, lines 1-33).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,228,678 to Gilleo et al. discloses pre-form underfills in which apertures are formed, and interface electrodes are disposed in the apertures.

b. U.S. Patent No. 6,228,681 to Gilleo et al. discloses methods for disposing interface electrodes inside apertures in underfill materials.

c. U.S. Patent No. 6,260,264 to Chen et al. discloses methods for exposing solder ball electrodes covered by an underfill material.

d. U.S. Patent No. 6,103,554 to Son et al. discloses carriers for holding singulated chips.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd
April 16, 2003

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
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